DAQ16 Device Specifications

V 1.25 04/23/20

System-on-Module (SOM) with RF analog I/O, Ultrascale+ RFSoC FPGA, 4GB Memory, QuadMesh Interlink

FEATURES

- Sixteen 12-bit A/D inputs
- Sixteen 14-bit D/A outputs
- 1000 mVp-p, direct-coupled, 50 ohm inputs
- 500 mVp-p, direct-coupled, 50 ohm outputs
- Xilinx Ultrascale+ ZU39DR RFSoC/FPGA
- 2 Banks of 64-bit, 2GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- External reference clock
- “Zero-phase error” external trigger
- Four, independent mesh links each providing 16 Gbps sustained transfer rates
- 4.0” x 5.0” SOM module.
- 40W typical power consumption
- Conduction cooled via cold-plate

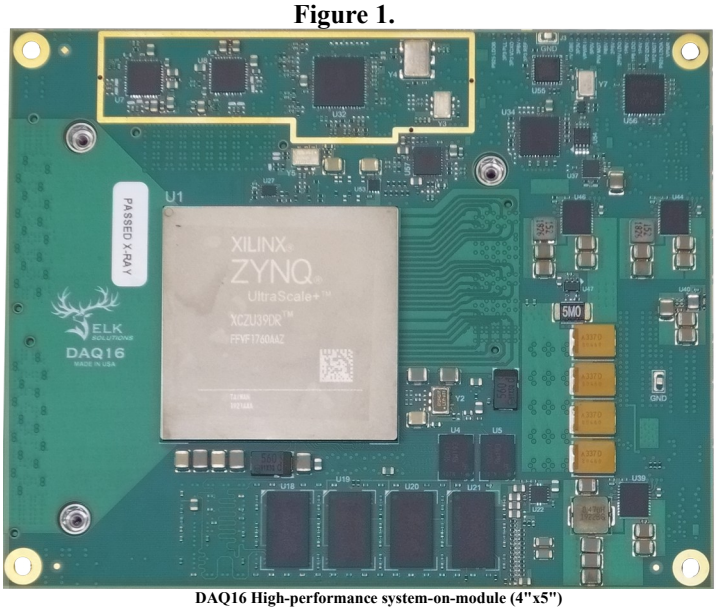
APPLICATIONS

- Beam steering
- WLAN, WCDMA, WiMAX front end
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- FrameWork Logic
- Petalinux Drivers
- C++ Host Tools

Figure 1.



DAQ16 High-performance system-on-module (4"x5")

DESCRIPTION

The DAQ16 integrates sixteen (eight IQ), digitizing channels and sixteen (eight IQ) waveform generation channels with real-time signal processing on a SOM IO module for demanding, real-time DSP applications. The tight coupling of the analog I/O within the Ultrascale+ RFSoC FPGA core provides low latency, optimized for architectures such as beam-steering, SDR, RADAR, and LIDAR front end sensor digitizing and processing. The Quad Mesh system interface sustains transfer rates at 16 Gbps to four peers concurrently facilitating creation of large meshes within high performance real-time systems.

The onboard 1760-pin Xilinx ZU39DR with 4 GB external DDR4 RAM addressable as two 64-bit banks, provides a very high performance DSP core. On-chip integration of multichannel, GSPS analog IO, zero-wait SRAM block memory and quad ARM CPU cores enable real-time signal processing at extremely high rates.

The DAQ16 exposes all sixteen of the RFSoC’s (6.5 GSPS-capable) D/A channels and sixteen (2.2 GSPS-capable) A/D channels. On chip mixer and interpolator/decimator capabilities (respectively) can be enabled to implement concurrent, real-time frequency conversions. Sample clocks are generated via a cascaded ultra-low-jitter onboard PLL referenced either via an onboard 10 MHz TCXO or externally-supplied reference clock. Phase aligned, synchronous sampling of all channels at full hardware rates across multiple cards is possible if supplied and external reference clock and trigger operating in the reference clock domain.

The DAQ16 can be fully customized using VHDL using the supplied board support package (BSP). The BSP provides standard IP cores for arbitrary waveform playback, and contiguous capture of ADC data of specified length (framed mode) DDR4 memory control and QuadMesh communications.

Software tools for target development include C++ libraries and drivers for Petalinux. Application examples demonstrating the module features and use are provided, including real-time, dynamic DAC waveform generation and analog captures.

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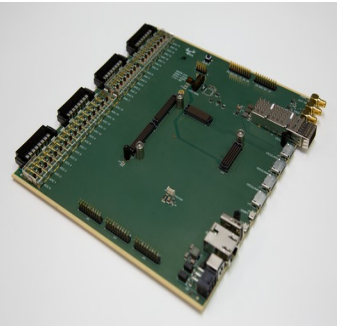
This electronics assembly can be damaged by ESD. Elk Solutions recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device to vary from published specifications.

ORDERING INFORMATION

Product	Part Number	Description
DAQ16	024000008-<CFG>-	  SOM module with sixteen, 12-bit 2.2 GSPS A/D, sixteen 6.5 GSPS 14-bit DAC, ZU39DR Ultrascale+ RFSoC, 4GB DRAM. <CFG> is configuration: 1 - Speed grade 1 FPGA
Single SOM carrier/breakout	024000006	 Left: IsoRate8 x 4 DAC0-15, DAC16-31, ADC0-15, ADC16-31 Right: Ref, TrigIn, TrigOut, QSFP28, PL Oculink4 x 3, PS Oculink 4 x 1, uUSB slave, uUSB JTAG, USB Host, 1 GbE, 2.5mm 6-16V, Samtec 6-16V, Top: PS DIO, Bottom: PL DIO, 8”x9”
Passive heatsink	008001113	 Thermal pad between RFSoC and heat spreader
Active Fansink	008001117	  Thermal pad between RFSoC and fansink assembly
DAQ16 FrameWork Logic	55012	DAQ16 board support package for VHDL.

DAQ16 Device Specifications

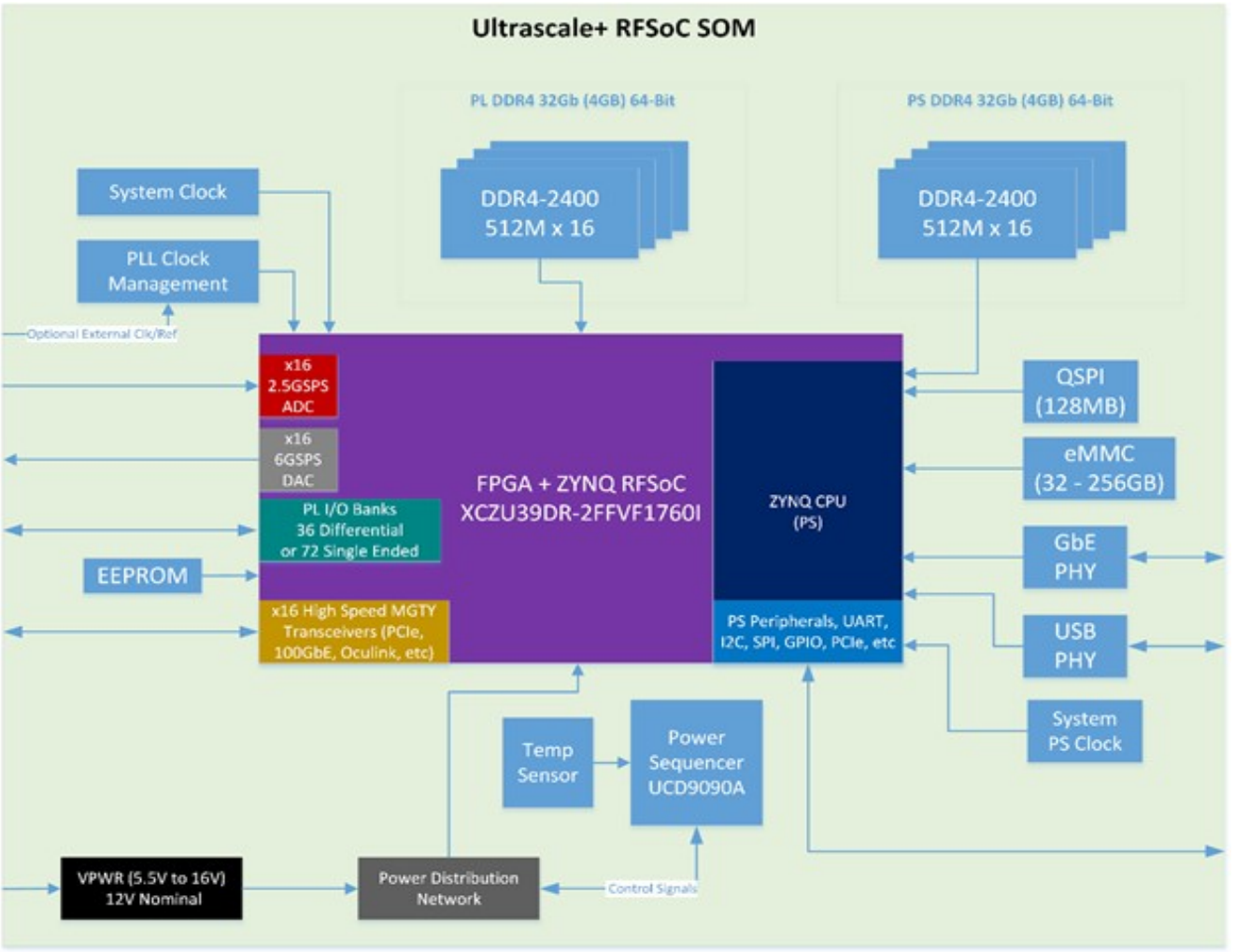


Illustration 2: Block diagram detail

Multiple-module synchronization: In order to achieve synchronous operation among multiple boards, all must be provided phase-aligned references. The reference feeds an onboard LMK04832 PLL which operates in nested zero-delay mode to guarantee it's outputs are phase aligned with the reference input. If a simple tunable oscillator were used instead, nested zero-delay mode would not be available and multi-board synchronous operation would not be possible.

The LMK can accept an external reference clock operating at up to 750 MHz. If the reference rate exceeds the FPGA SYSREF clock rate (which is limited to < 10 MHz), a phase-aligned synchronization pulse must be presented to the LMK SYNC pin to phase align the LMK outputs of all boards in the system. This is essential to phase-aligned analog I/O across modules. Elk has exposed the LMK SYNC pin from the SOM for this very purpose. If the reference clock rate is less than 10 MHz, the LMK SYNC pin may be ignored.

A low-jitter, high-stability, external reference must be supplied to all modules operating at an integer submultiple the greatest common divisor of 16 and the chosen ADC and DAC sample rates.

DAQ16 Device Specifications

The onboard LMK PLL produces a lower-jitter SYSREF identical in rate and phase to EXT REF plus phase-aligned ADC sample or reference clocks. The LMK is limited to 3.02 GHz but has some coverage gaps. The onchip RF tile PLLs are automatically used if the requested ADC sample rate falls outside of the LMK coverage range. The LMX PLL can produce a sample clock covering the entire DAC operational range so it's always used to synthesize the DAC sample clock.

The diagram below is an excerpt from the LMK04832 datasheet.

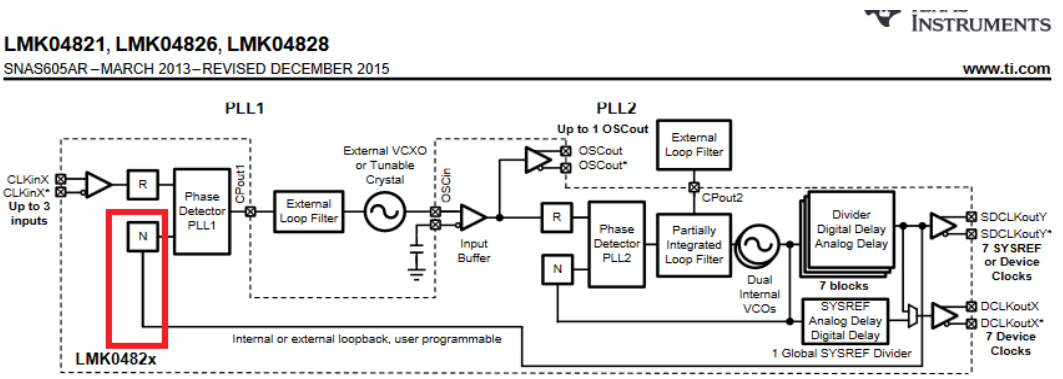


Figure 19. Simplified Functional Block Diagram for Nested 0-delay Dual Loop Mode

The LMK employs a feedback loop to insure that the output frequency (SDCLKout/DCLKout) remains synchronous to the input reference clock (CLKin). An integer divider N (highlighted) is present in the feedback path, capable of dividing the output frequency by any integer (1-8192) to match the input frequency if needed to close the feedback loop.

The LMK is used on the DAQ16 to generate the SYSREF signal used by the RFSoC as the timing reference for the ADC and DAC subsystem. Xilinx imposes the following restrictions on SYSREF:

SYSREF Signal Requirements

The SYSREF signal is the timing reference for the system and must therefore be handled correctly to ensure it does not degrade the synchronization. This signal has the following requirements.

1. The SYSREF signal must be a high-quality, free-running, low-jitter square wave, to allow it to be captured consistently by the analog sample clock.
2. The SYSREF frequency must meet the following requirements:
   a. If synchronizing RF-ADC and RF-DAC tiles with different sample frequencies, the frequency must be an integer submultiple of:

      GCD(DAC_Sample_Rate/16, ADC_Sample_Rate/16)

   b. SYSREF must also be an integer submultiple of all PL clocks that sample it. This is to ensure the periodic SYSREF is always sampled synchronously.
   c. Less than 10 MHz.

In summary, the external reference supplied to the DAQ16 must be a sub-multiple of 16 and the chosen sample rates. If the external reference rate is greater than 10 MHz, a SYNC pulse must further be provided to all cards in the system to avoid phase indeterminacy.

Triggering: External trigger (EXT TRG) must operate in external reference (EXT REF) time domain. It must be marshaled into the external reference domain via a flip-flop that is clocked by SYSREF. This function can be performed by one of the DAQ16 cards acting as master. ADC/DAC samples flow via the RFdc core in clumps (each 8, 16 or 32 samples (user-defined)), at an LMK-generated FSCLK rate of 200-400 MHz. Consequently, the synthesized multi-board synchronous trigger must reliably fall within a 1/ FSCLK window on all cards, which is readily achievable.

DAQ16 Device Specifications

Standard Features

Analog Inputs	
Channels	16
Range	700 mVp-p (typical)
Type	Differential
Coupling	DC
Impedance	50 ohm (typical)
A/D Device	RFSoC internal
Resolution	12-bit
Sample Rate	100-2200 MSPS.
Impedance	50 ohm +/- 1 ohm
Prog. Bias	N/A
FIFO size	128K for each active channel
Data transfer	RFdc driver
Connectors	Samtec SEAM8 30x8 female
Clocking	All ADCs synchronous. Integer fraction of DAC rate.

Analog Outputs	
Channels	16 channels
Range	700 mVp-p (typical)
Type	Differential
Coupling	DC
Impedance	50 ohm (typical)
D/A Device	RFSoC internal
Resolution	14-bit
Sample Rate	100-6500 MHz.
Impedance	50 ohm +/- 1 ohm
Prog. Bias	N/A
FIFO size	128K for each active channel
Data transfer	RFdc driver
Connectors	Samtec SEAM8 30x8 female
Clocking	All DACs synchronous. Integer multiple of ADC rate.

DAQ16 Device Specifications

Standard Features

Analog Trigger In	
Source	SEAM40 connector, Software
Functions	Start Trigger, Start Frame
Source Level	0-3.3V, active at 1.8V typical
Modes	Edge, Level
Pulse width	6 min, 50 max (nS)
Accuracy	+/- 0 samples when trigger source and reference clock in same domain
Impedance	50 +/- 1 ohm
Coupling	DC
Protection (power on, off)	+/- 4V, +/- 2V
Impedance	1 Mohm
Latency	Assert trigger on following SYSREF edge

Analog Trigger OUT	
Source	SEAM40 connector, Software
Functions	Start Trigger, Start Frame
Source Level	0-1.8V
Modes	Pulse
Pulse width	6 min, 50 max (nS)
Impedance	50 +/- 1 ohm
Coupling	DC
Impedance	50 ohm

Phase Locked Loop	
Number of PLLs	3
Tuning resolution/ restrictions	ADC: See LMK04832 datasheet DAC: See LMX2594 datasheet
Reference Frequency	10-100 MHz. 3.3V CMOS signal levels.
Reference Source	SEAM40 HD connector pin or onboard osc
Clock Sources	Ext. or Int. TCXO
	External Inputs: 0 dBm nominal AC-coupled, 50-ohm terminated, SMA
Jitter	Internal: <100 fs rms
Channel Clocking	All channels are synchronous
Multi-card Synch	Must phase lock to external 10-100 MHz system reference (SYSREF) using nest 0-delay mode. 3.3V CMOS signal levels.

DAQ16 Device Specifications

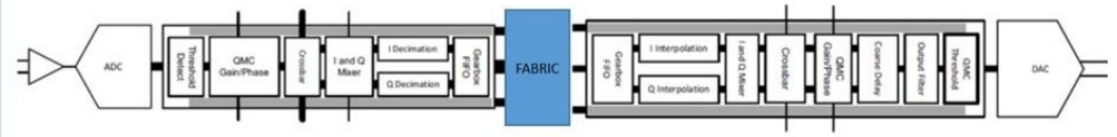
Standard Features

FPGA	
Device	Xilinx Ultrascale+ RFSoC XCZU39-1FFVG1760E or I. See Xilinx document DS889 v1.8, Table 9 for environmental options
Speed Grade	-1 (extended temp)
System Logic Cells	930,000
CLB LUTs	425,000
Maximum Distributed RAM (Mb)	13
Block RAM (Mb)	38
UltraRam (Mb)	22.5
GTY Transceivers	16 (all exposed to carrier)
Configuration	Two Micron MT25QU512ABB8E12-0SIT TR QSPI flash EEPROM. JTAG during development

Memories	
DRAM Size	4 GB total 8 devices @ 256Mb x16 each
DRAM Type	DDR4 DRAM
DRAM Controller	Controller for DRAM implemented in logic. Each 64 bit interface uses 2.5 FPGA I/O banks, 10@ 13 bit FPGA I/O Byte lanes (4 per bank).
Total DRAM Bandwidth	38.4GB/s maximum bandwidth (100% data bus efficiency, applications' efficiency varies)

Flash Disk	
eMMC Size	Sandisk 'SDINBDG4-32G-XI1 device provides 32 GB of NV storage.

Figure 2.



RFSoC Digital processing configuration	Latency (Sample Clocks)	Latency ns(FS=6.4GSPS)	Latency ns (FS= 4GSPS)
DAC Datapath-all digitalfeature bypass (Min config)	160	25	
DAC / 8x Interp, Inv-Sinc, NCO, QMC, ProgFilt(Max config)	762	119	
ADC Datapath-all digitalfeature bypass (Min config)	188		47
ADC / 8x Decim, NCO, QMC (Max config)	412		103
ADC Analog front end & calibration	95.54		23.89
NCO and QMC together	72	11.25	18
Decimation or Interpolation x8	360	56.25	90
Decimation or Interpolation x4	200	31.25	50
Decimation or Interpolation x2	96	15	24
Decimation or Interpolation bypass	16	2.5	4

RFSoC Latency operating at uniform 1 GSPS

DAQ16 Device Specifications

Standard Features

Monitoring	
Alerts	Firmware-specific. Typically, Trigger Start, Trigger Stop, Queue Underflow, Timestamp Rollover, Temperature Warning and Failure. 32-bit counter with rollover and resolution is 1 analog sample.

Digital IO	
Number of pins	72
Signal Standards	FPGA 1.8V HIGH RANGE (LVCMOS18 default see Xilinx select IO user guide UG571) DIO routed as differential pairs
Connector	Samtec SEAM8 connector

SoC I/O	
Ethernet (1 GbE)	Signals upstream of phy on carrier
USB	1 root, 1 slave
MGT	8 x 25 Gbps
JTAG	14 pin JTAG (2mm pitch on carrier)
Connector	Samtec SEAM8 connector

Power	
Consumption	5.5-16Vdc (45 Watts typical)
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling to chassis coldplate or heatsink

Physicals	
Form Factor	Custom
Size	101x127mm
Weight	156g
Hazardous Materials	Lead-free and RoHS compliant

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Analog Performance At 24C ambient.			
Parameter	Typ	Units	Notes
A/D Performance – AC coupled			
Analog Bandwidth	3000	MHz	-3dB.
SFDR	83 75	dBc	71 MHz sine input, 95%FS, Fs = 4.0 GSPS 220 MHz sine input, 95%FS, Fs = 4.0 GSPS
S/N	56	dBFS	170 MHz sine input, 98%FS, Fs = 1.0 GSPS
SINAD	57	dBFS	170 MHz sine input, 95%FS, Fs = 1.0 GSPS
ENOB	9.3	bits	170 MHz sine input, 98%FS, Fs = 1.0 GSPS
Channel Crosstalk	-55	dB	Typical @ -1 dBm, 2.26 GHz CW sine (aggressor) on adjacent channel and Fs = 1966.08 MSPS
Noise Density	-132	dBm/Hz	Input grounded, Fs = 1.0 GSPS, 64K sample FFT, non-averaged
Gain Error	<1%	% of FS	Calibrated
Offset Error	<1	mV	Calibrated
DAC Performance – AC Coupled			
Analog Bandwidth	3000	MHz	-3 dB
SFDR	78 70	dBc	71 MHz @ -9 dBFS, 1000 MSPS sample rate 170 MHz @ -9 dBFS, 1000 MSPS sample rate
IMD	-80 72	dBc	71 MHz @ -9 dBFS, 1000 MSPS sample rate 170 MHz @ -9 dBFS, 1000 MSPS sample rate
ENOB	9.5	bits	71 MHz sine output, AC coupled
Noise spectral density	-145	dBm/Hz	170 MHz @ 0dBFS, 1000 MHz sample rate
Channel Crosstalk	-55	dB	Aggressor = 710 MHz, -1 dBfs adjacent channel
Gain Error	<1 %	% of FS	Calibrated
Offset Error	<500	µV	Calibrated

DAQ16 Device Specifications

Architecture and Features

The DAQ16 module architecture incorporates a Ultrascale MPSoC system-on-chip which incorporates quad ARM processors and dual real-time coprocessors, FPGA computing core, on chip RF analog I/O and Aurora QuadMesh core. These resources are integrated with external DDR4 external memories, ultra-low jitter programmable sample clock, boot flash and power management. The resulting architecture tightly couples the programmable FPGA fabric for real-time signal processing to the RF analog I/O with low latency and extremely high rates.

Analog IO

The ZCU39 RFSoC device provides sixteen A/D and D/A channels internally. All A/D D/A channels are exposed via connectors on the DAQ16 SOM. Samtec IsoRate connectors are used to preserve the wide analog bandwidth for use in wideband and direct sampling applications.

The ADC and DAC devices are implemented directly on the FPGA die replacing gigabit transceiver tiles and are directly addressable by the logic fabric. In the standard logic provided in the BSP, the A/Ds have an interface component that receives the data, provides digital error correction (y=mx+b linearization), and a FIFO memory for buffering. The trigger manager within the firmware affords precise control over the collection of data. Trigger modes include frames of programmable size, continuous, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized in the logic to accommodate new triggering requirements, should they arise. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.

FPGA Core

The DAQ16 employs a Zynq Ultrascale+ RFSoC for DSP and control. This system-on-chip FPGA is capable of over 8.2 TeraMACs with over 4200 DSP elements. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to one 64-bit bank of DDR4 RAM. This memory allows the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. An Axi DMA multiple-queue controller component will be used to coordinate multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

All IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the module functionality. Logic utilization of the standard Framework Logic is <15% of the device.

QuadMesh Host Interface

The DAQ16 architecture delivers ~ 64 Gbps sustained data rates over QuadMesh using the Aurora protocol. Packet systems can be implemented atop Aurora as an application interface layer to provide efficient, flexible inter-board transfers at high data rates. Typical packet data systems control the flow of packets using a credit system managed in cooperation with the mesh supervisor software.

The module has 16 high speed serial data links present on the HD connector. These are exposed via OcuLink connectors on the expansion carrier for system interconnect, operating at up to 16 Gbps per link, full duplex. These links enable modules to integrate into switched fabric systems to create powerful computing and signal processing architectures. The standard logic uses these lanes as two bonded Aurora ports of 2 lanes each. Other protocols such as sFPDP could be implemented in the FPGA.

Digital IO

48 digital lines are routed directly from the FPGA as length-matched differential pairs. These signals originate in the I/O FPGA banks, supporting operation conformant with the 1.8V I/O standard. These are useful for implementing low-latency state signaling, or interfacing to custom hardware devices via I2C, SPI or other common serial or parallel standards. 24 additional digital lines are routed from the PS as length-matched single-ended 3.3V signals.

DAQ16 Device Specifications

Module Management

The module has facilities for temperature monitoring within the FPGA die. The temperature sensor is monitored by a dedicated system monitor IP, so that power shuts when a critical temperature is exceeded. This function is independent of the FPGA but resident on-chip.

FPGA Configuration

The module uses a QSPI parallel FLASH memory to configure the Ultrascale+ RFSoC FPGA image. This FLASH can be programmed in-system using a supplied software applet.

During development, the JTAG interface to the FPGA may be used for development tools. The FPGA JTAG connector may be controlled using inexpensive USB Digilent debug aids providing compatibility with the Xilinx Platform USB Cable. However more commonly and conveniently, the target may boot PetaLinux and an ethernet connection used to facilitate in-system debugging via the Xilinx target communication framework (TCF).

DAQ16 clocking topology

The DAQ16 supports heterogeneous ADC/DAC rates as shown in the figure below.

Figure 3.

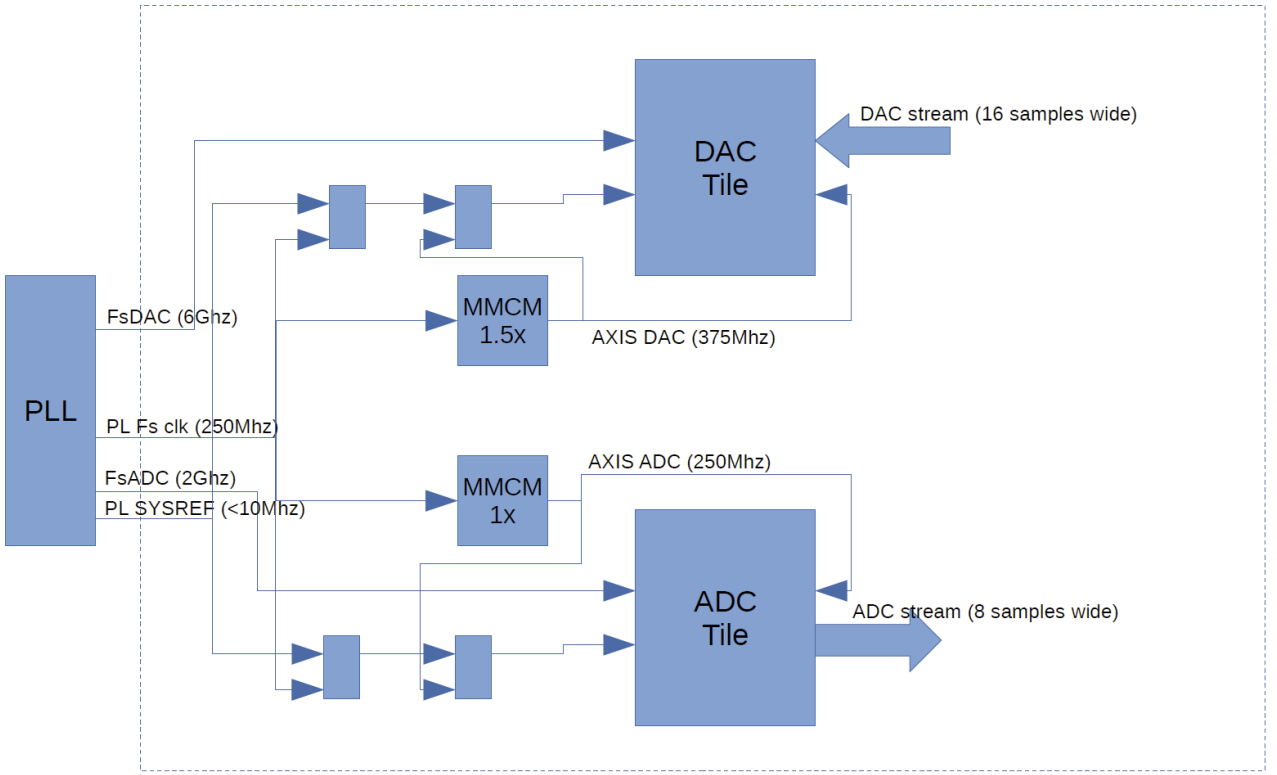

Figure 1: Clocking topology

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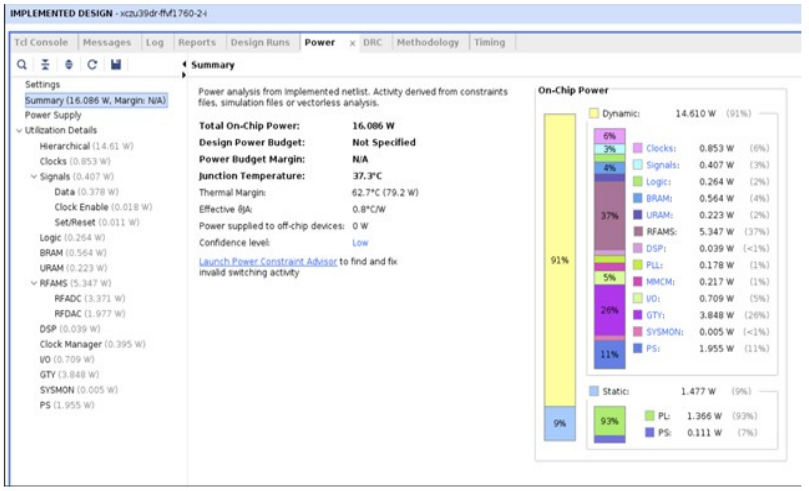
The DAQ16 employs three PLLs to synthesize various clocks needed throughout the system. The first stage PLL is an LMK04832 which integrates two VCOs. Nine outputs from this PLL are used as follows:

Output	Purpose
0	ADC_225_CLK (Tile1)
2	ADC_224_CLK (Tile0)
4	ADC_227_CLK (Tile3)
6	ADC_226_CLK (Tile2)
7	SYSREF_PL
8	LMX_2594B (Reference to LMX, which clocks DAC tiles 2, 3)
10	LMX_2594A (Reference to LMX, which clocks DAC tiles 0, 1)
12	FS_CLK (FPGA state machine clock which services ADC and DAC tiles)
13	SYSREF_IN

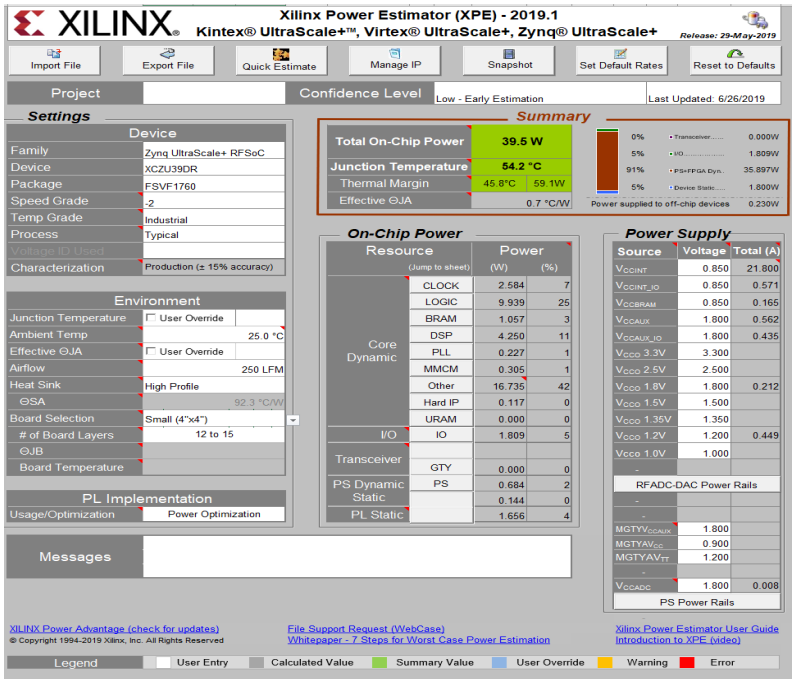
DAQ16 Device Specifications



Power Dissipation

Power dissipation is heavily dependent on the firmware implementation. Typically, using more SERDES channels, more ARM cores and enabling RFdc core will increase power consumption.

The Xilinx power estimator for the supplied firmware design predicts baseline module power consumption to be approximately 16W and to increase modestly when either the the SERDES or RFdc cores are switched at full frequency.



Ironically, the Xilinx power estimator for the same design predicts 39.5W on-chip power use.

The Xilinx tools have many "knobs and levers" that can be adjusted, definitively indicating that the power consumption will range somewhere between **16 and 40W**! Obviously, that's a very wide range and these tools are insufficient to help plan your design.

When generating sine waves on all DACs and capturing from all ADCs, the SOM+carrier draws

Voltage at test point VPWR I: 0.26V
Current = (VPWRI/20)/.005 = 2.6A
Supply Voltage: 12.17V
Power = IV = 2.6A * 12.17V = **31.64W**

The RFSoCs report a die temperature of ~55C throughout the test, with the active heatspreader attached. But bear in mind that none of the Aurora channels were in use during that test.

Software Tools

Software development tools for the module provide comprehensive support via C++ libraries, including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the outset. At the most fundamental level, the software tools deliver data buffers to application code without the burden of low-level real-time control of the cards. Software classes provide a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Support for the GNU C++ toolchain is provided by the Xilinx SDK. The target ARM processors run a 64-bit variant of Petalinux, source for which is supplied within the BSP.

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Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the module by modifying the logic. The Board Support Package (BSP) tool provides support for RTL development. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the BSP is provided for customization. Each design is provided as a Xilinx Vivado project, with a testbench illustrating logic functionality.

DAQ16 Device Specifications

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